

**DIRECT IMPLANTATION OF FLUORINE INTO THE
CHANNEL REGION OF A PMOS DEVICE**

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TECHNICAL FIELD

 The present invention relates to the implantation of fluorine directly into the channel
 region of a PMOS transistor structure to improve the $1/f$ noise and V_T drift margin of the
15 device performance.

BACKGROUND OF THE INVENTION

 Mixed signal integrated circuits find the option of dual (or more) gate oxide processes
 attractive in that multiple voltages can then be used on the same chip. This technique
20 requires that gate oxides be grown twice, to result in different gate oxide thicknesses, and
 often with different well implantations, so as to provide optimal performance for both the
 high voltage and the low voltage transistors.

 Hook et al., "The Effects of Flourine on Parametrics and Reliability in a 0.18um
 3.5/6.8 nm Dual Gate Oxide CMOS Technology", IEEE Transactions on Electron Devices,
25 Vol. 48, No. 7, July 2001, pp. 1346-1353, discuss the benefits of the introduction of fluorine
 into gate oxide by implantation into the gate polysilicon in PMOS devices.

 For reasons of mask count reduction, and thus cost, it is attractive to make use of
 common source-drain implants, spacer formation and silicidation processing, which are
30 common to both high and low voltage transistors.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a cross section drawing illustrating a conventional PMOS transistor structure.

Fig. 2 is a cross section drawing illustrating the Fluorine profile in a conventional PMOS transistor structure.

5 Figs. 3A-3D provide a sequence of cross section drawings illustrating a method of fabricating a PMOS transistor structure with a Fluorine-doped channel region in accordance with the present invention.

DETAILED DESCRIPTION

10 High voltage PMOS transistors are known to be susceptible to threshold voltage (V_T) drift, gate induced drain leakage (GIDL), and trap induced noise ($1/f$). The present invention utilizes the implantation of fluorine directly into the channel region of the PMOS transistor, at the time that an N-well implant stack is processed, for example, to improve the analog performance of the high voltage PMOS device without an additional mask cost.

15 Fig. 1 shows a conventional PMOS transistor structure 10 formed in N-type semiconductor material 12, typically silicon. The PMOS structure 10 includes a P-type source region 14 and a P-type drain region 16 formed by the introduction of P-type dopant into the N-type semiconductor material 12. The polysilicon gate electrode 18 of the PMOS device is separated from the channel region 20 by intervening gate dielectric material 22, e.g.
20 silicon dioxide. Fig. 1 illustrates one conventional method of introducing P-type dopant into the semiconductor material 12 by utilizing the poly gate 18 for the self-aligned ion implantation of BF₂; utilizing BF₂ provides for the diffusion of fluorine into the edges of the channel region 20, i.e. the circled regions in Fig. 1, to somewhat improve the GIDL and trap induced noise issues mentioned above. Fig. 2 shows the fluorine profile in the PMOS
25 structure 10 resulting from utilizing BF₂ in a self-aligned implant. As discussed in the Hook et al. publication, the presence of Fluorine in the gate poly 18 and the gate oxide can foster Boron migration through the gate oxide, thereby impacting on the reliability of the device. Boron diffusion or penetration through the gate oxide can lead to lessened control of the threshold of the device and related channel leakage. As Fluorine in the gate oxide is known
30 to increase the diffusivity of the Boron, there therefore exists a device design preference to keep Fluorine out of the gate oxide to a greater extent than is the case when high dose BF₂

source/drain implants are used. A dose of Flourine, implanted deeper into the channel, but still close enough to the surface to passivate traps, will thus gain the benefits of both lessened boron penetration and Flourine-based trap passivation.

5 Figs. 3A-3D show one sequence of steps that can be utilized to fabricate a PMOS transistor structure in accordance with the concepts of the present invention.

Fig. 3A shows a conventional shallow trench isolation (STI) structure 102 formed in a semiconductor substrate 100. In the illustrated embodiment, the semiconductor substrate 100 is P-type silicon. The upper surface of the active device region defined by the STI structure 102 is exposed by an opening formed in patterned photoresist mask (PR) 104. An N-well 106 has been formed in the active region utilizing conventional techniques. Fig. 3A also shows the formation of an optional n+ threshold adjustment region 108 using the same mask structure utilized to form the N-well 106. In accordance with the concepts of the present invention, the same mask structure utilized to form the N-well 106 (and, optionally, the Vt adjustment region 108) is for the ion implantation of Flourine directly into an upper surface area 110 of the N-well 106.

Fig. 3B shows that, following the removal of the PR mask 104, a layer of gate dielectric material 112, e.g. thermally grown silicon dioxide, is formed on the upper surface of the N-well 106. As shown in Fig. 3C, a layer of undoped (???) polysilicon 114 is then formed on the gate dielectric material 112 by well-known methods.

Referring to Fig. 3D, utilizing conventional techniques, the poly layer 114 is then masked and a stacked gate etch is performed to define a poly gate electrode 116 that is separated from the N-well 106 by intervening gate oxide 118. P-type dopant, e.g. BF₂ or B, is then introduced into the N-well 106 at the sides of the poly gate 108 in a self-aligned ion implant step that results in the formation of P-type source (S) region 120 and P-type drain (D) region 122 to complete this embodiment of a PMOS transistor structure.

Of course those skilled in the art will appreciate that the key feature of the fabrication method disclosed above is the introduction of Flourine into the channel region of the PMOS device, and not the particular sequence of steps for its fabrication or the specific details of its final structure. Other fabrication sequences and PMOS device structures are contemplated as being within the scope of the invention. By way of example, not limitation, the concepts of

the invention include implanting Flourine through a sacrificial oxide prior to clean and gate oxide growth, implanting Flourine through the gate oxide into the channel region below, and, after poly gate metal etch, implanting Flourine at an angle similar to that of a conventional halo implant and at the same time as a halo implant so as to angle the dose into the source-drain/gate overlap regions.

The use of Flourine implantation directly into the channel region of a PMOS transistor improves the noise and V_t drift margin of device performance by introducing Si-F complexes at the interface between the N-well Silicon and the gate oxide. Importantly, this technique avoids additional issues typically associated with the use of Flourine; namely, Flourine is known to raise the diffusivity of Boron in oxides and, hence, can lead to penetration of boron from poly gates into the channel region for the case of thin oxides.

It is believed that the concepts disclosed above will not work as effectively for N^+ on P- diodes since, as mentioned in the Hook et al. publication, traps in the upper half of the bandgap will increase in these structures with the introduction of Flourine.

Although only specific embodiments of the present invention are shown and described herein, the invention is not to be limited by these embodiments. For example, Deuterium, rather than Flourine, can be used with similar results. Rather, the scope of the invention is to be defined by these descriptions taken together with the attached claims and their equivalents.